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(54) [Title of the Invention] THIN FILM TRANSISTOR AND MANUFACTURING METHOD THEREOF

(57) [Abstract]

[Object] Low melting point glass can be used and lowering cost of a device is attained by setting a temperature of a manufacturing process of a polycrystalline silicon thin film transistor to be 450°C or less. In addition, enhancing electron field-effect mobility of a

thin film transistor is attained by setting crystal orientation of polycrystalline silicon to have preferred orientation of {110} orientation.

[Structure] Preferred oriented polycrystalline silicon of {110} orientation is deposited at a substrate temperature of from 200 to 300°C over a glass substrate by diluting gas containing silicon with a high flow of a hydrogen gas and then depositing by a plasma CVD method. A thin film transistor is formed with this polycrystalline silicon thin film.

[Effect] A polycrystalline silicon thin film can be formed at a substrate temperature of approximately 200°C; therefore, there is an extraordinary effect on lowering cost of a device to which a thin film transistor is applied. In addition, in a method of the present invention, a halogen-based etching gas is not used; therefore, an impurity which causes deterioration of a device characteristic is not mixed into a film. Furthermore, depositing is performed in hydrogen gas plasma; therefore, a high-performance polycrystalline silicon thin film transistor can be manufactured without a requirement of hydrogen passivation after depositing.

[Scope of Claims]

[Claim 1] A thin film transistor using polycrystalline silicon formed over an amorphous substrate as its major portion, characterized in that the polycrystalline silicon has a preferred orientation in which a crystal orientation is {110} orientation.

[Claim 2] A manufacturing method of a thin film transistor over the amorphous silicon substrate, characterized in that the polycrystalline silicon is made by a plasma chemical vapor deposition method.

[Claim 3] The manufacturing method of the thin film transistor according to Claim 2, characterized in that all steps are carried out at 450°C or less.

[Claim 4] The manufacturing method of the thin film transistor according to Claim 2, characterized in that a channel region of the thin film transistor is formed by a plasma chemical vapor deposition method.

[Claim 5] The manufacturing method of the thin film transistor according to Claim 2, characterized in that a source/drain region of the thin film transistor is formed by a plasma chemical vapor deposition method.

[Detailed Description of the Invention]

[0001]

[Industrial Field of the Invention] The present invention relates to a thin film transistor, especially a manufacturing method of a polycrystalline silicon thin film transistor.

[0002]

[Prior Art] An attempt to make a thin film transistor (TFT), in which microcrystal or polycrystalline silicon (poly-Si) is used as an element material, over low melting point glass is activated. Especially, a process for making a TFT having high mobility and high ON/OFF ratio at a highest temperature of a process of 450°C using a low melting point glass substrate such as a 7059 substrate manufactured by Corning Incorporated as a substrate is expected to be put into practical use.

[0003] Conventionally, a method for thermally decomposing a monosilane gas at a substrate temperature of approximately 600°C by a low pressure CVD method is known to deposit poly-Si over a glass substrate. In addition, there is a method for making a

TFT by forming poly-Si in which the grain diameter of amorphous Si (a-Si) is enlarged by a solid-phase growth method or a method for making a TFT by melting and recrystallizing a-Si or poly-Si by laser annealing as a conventional method for making a high-performance poly-SiTFT.

[0004]

[Problems to be solved by the Invention] However, as for poly-Si by a low pressure CVD method, low melting point glass cannot be used for a substrate owing to a depositing temperature. Further, low melting point glass cannot be used for a substrate also in a method for obtaining poly-Si having a large grain diameter by a solid-phase growth method since annealing has to be performed for a long time from 4 to 70 hours at a temperature of approximately 600°C. Laser annealing has problems such as variation of an element characteristic due to a nonuniform characteristic of a laser beam and low throughput.

[0005] Therefore, a method, which can manufacture polycrystalline silicon at a low temperature by performing glow discharge decomposition on a mixed gas of a silane gas and an etching gas such as fluorine or phlorosilane (fluorosilane だと思う) by a plasma chemical vapor deposition method (PCVD), attracts attention as shown in Patent Laid-Open No. S63-175417; Patent Laid-Open No. H2-177368; Patent Laid-Open No. H2-202018; MaterialsResearch Society Simposia Proceedings, Volume 95, p. 225 (1987); or the like.

[0006] A poly-Si thin film obtained by these deposition methods contains a halogen gas such as a fluoride gas or a halide such as fluorosilane or dichlorosilane as an etching gas; therefore, a halogen atom such as fluorine or chlorine is contained as an impurity in poly-Si which is obtained. When a poly-SiTFT is produced, these impurities cause a crystalline defect and become a critical problem because a leak current of a TFT increases.

[0007] The invention solves the above problem, and its object is to provide a high-performance poly-SiTFT made over low melting point glass and a manufacturing method thereof.

[0008]

[Means for solving the Problems] A thin film transistor of the present invention using polycrystalline silicon formed over an amorphous substrate as its major portion is characterized in that the polycrystalline silicon has a preferred orientation in which crystal orientation is a {110} orientation.

[0009] A manufacturing method of a thin film transistor over the amorphous silicon substrate is characterized in that the polycrystalline silicon is made by a plasma chemical vapor deposition method.

[0010]

[Example] Hereinafter, a manufacturing method of the invention is described in detail. A substrate which is to be used may be low melting point glass, a ceramic substrate, or the like, or a quartz substrate, other than a substrate of single crystalline Si. When single crystalline Si is used for the substrate, an epitaxial Si film can be obtained, not poly-Si. In this example, a 7059 substrate manufactured by Corning Incorporated is used. The substrate is not limited to the 7059 substrate, and any kind of substrates such as a quartz substrate, which can withstand a process temperature of approximately 450°C, may be used. First, a doped poly-Si thin film which is to be a source region 101 and a drain region 102 is deposited to be from 2000 to 3000 Å by a PCVD method over a substrate 100. An object in which a doping gas is added to an object in which a silane gas is diluted with a hydrogen gas is used as a deposition gas. For example, in the case of n-type poly-Si, phosphine, arsine, or the like is used as a doping gas, and in the case of p-type poly-Si, diborane or the like is used. In this example, phosphine is used in the case of n-type, and diborane is used in the case of p-type. The flow ratio of gas is SiH_4: H_2: PH_3=1.800: 98.191: 0.009 in n-type, and SiH_4: H_2: B_2H_6=1.800: 98.164: 0.036 in p-type. Total flow of gas is 200 SCCM in both of n-type and p-type. Doped poly-Si is deposited using this deposition gas by PCVD in the similar way to that of depositing channel poly-Si described hereinafter. In a doped poly-Si which is obtained, the sheet resistance of n-type having a film thickness of 2000 Å is 300 Ω/□ and p-type having a film thickness of 3000 Å is 500 Ω/□; and thus, low resistance can be obtained. After depositing the doped poly-Si, patterning is carried out into a form of the source region 101 and the drain region 102 (FIG. 2-(a)).

[0011] Subsequently, channel poly-Si is deposited to have a film thickness of from 200 to 1500 Å by a PCVD method again. PED-302 type manufactured by ANELVA corporation having a parallel-plate type electrode is used for a PCVD device which deposits poly-Si. Hereinafter, a method for depositing poly-Si is described. FIG. 1 shows a schematic view of the PCVD device used in the invention. 1 denotes a reaction chamber, 2 denotes an exhaust duct, 3 denotes a counter electrode, 4 denotes a gas-blowout hole, 5 denotes a gas-introducing portion, 6 denotes a high frequency application electrode, 7 denotes a heater for heating substrate, 8 denotes a substrate, and 9 denotes a high frequency power source. W in FIG. 1 denotes a distance between electrodes. A mixed gas of H_2 and SiH_4, Si_2H_6, Si_3H_8, or the like is used for a deposition gas. In this example, a mixed gas of SiH_4 and H_2 is used.

[0012] Basic reaction mechanism follows formula 1 shown next. In reaction of formula 1, R1 denotes deposition reaction and R2 denotes etching reaction.

[0013]

[chem. 1]

$$SiHn\ (plasma) \underset{R2}{\overset{R1}{\rightleftharpoons}} Si\ (solid) + nH\ (plasma) \qquad \text{(formula 1)}$$

(n denotes a dimensionless number) In formula 1, the reaction of R2 becomes dominant when a hydrogen concentration increases; therefore, a Si-H bond which has low bond energy is selectively cut by the etching reaction of R2. Therefore, only a Si-Si bond remains and poly-Si is deposited over the substrate on such a condition. On the other hand, the deposition reaction of R1 in formula 1 becomes dominant when a silane gas concentration increases, and amorphous silicon (a-Si) having high hydrogen concentration is deposited over the substrate. Such a competitive relation between R1 and R2 can be easily adjusted by changing the ratio of silane gas concentration to hydrogen gas concentration. Therefore, it is required that the ratio of silane concentration/hydrogen concentration is set to be at least 0.1 or less by diluting a silane

gas with a high flow of a hydrogen gas to form a poly-Si thin film.

[0014] In the case of practically depositing poly-Si, the concentration ratio of silane/hydrogen gas is desirably SiH_4/H_2=from 0.5 to 5.0%, especially from 1.0 to 3.0% in gas flow ratio. If the ratio is smaller than 0.5%, the etching reaction by a hydrogen gas becomes too dominant, the deposition rate becomes extremely low, and only poly-Si having a small grain diameter is deposited. If the ratio is larger than 5.0%, deposition reaction becomes dominant and only a-Si is deposited.

[0015] The pressure in the reaction chamber is from 0.1 to 10.0 Torr, and especially, from 0.3 to 1.5 Torr is preferable. High frequency electric power which generates plasma is set to have an electric power density of from 0.01 to 5.0 W/cm^2, preferably from 0.03 to 0.06 W/cm^2. If the power density is lower than 0.01 W/cm^2, the etching reaction becomes too weak. If the power density is higher than 5 W/cm^2, a high-quality film cannot be formed since a thin film is subject to a plasma damage. A substrate temperature is from 100 to 450°C, preferably from 200 to 400°C. When a substrate temperature is lower than 100°C, a-Si is deposited, and when higher than 450°C, it exceeds allowable temperature of the 7059 substrate used in this example, and advantage of low temperature deposition PCVD cannot be taken.

[0016] An important condition of depositing poly-Si is a distance between opposite electrodes of a parallel-plate type PCVD apparatus (hereinafter, referred to as a distance between electrodes; W in FIG. 1). The distance between electrodes has to be sufficiently short and hydrogen has to reach the substrate in an active state in order to promote the etching reaction. In the case where the distance between electrodes is long, the etching reaction is developed in a gaseous phase and amorphous silicon is deposited over the substrate. Therefore, the distance between electrodes W is defined by a high frequency electric power and a pressure. In the case where the high frequency electric power is 0.03 W/cm^2 and the pressure is 1.2 Torr, the distance between electrodes W is required to be less than 45 mm, preferably 27 mm or less, and more preferably 20 mm or less. In this example, W is set to be 20 mm. Before depositing, a mixed gas of SiH_4: H_2=1.8: 98.2 is supplied to the reaction chamber of vacuum of 1×10^{-6} Torr or less in a total flow of 200 SCCM, and inner pressure is

adjusted to be 1.2 Torr. After setting a substrate temperature to be 230°C, a deposition gas is flowed for approximately 20 minutes until stabilizing a substrate temperature. Then, a discharge is performed for 44 minutes with discharge electric power of 0.03 W/cm^2 with the use of high frequency power source of 13.56 MHz to grow a silicon thin film in approximately 1000 Å over the 7059 substrate. In addition, conventionally, a particle is generated when a-Si or the like is deposited by a PCVD method and this had heavily caused lowering of yield of a TFT device. However, a particle is merely generated by the manufacturing method of the invention; therefore, there is an extraordinary effect on enhancing yield of a TFT device.

[0017] In the deposition method by a PCVD method of the invention, it is clarified from a measurement of X-ray diffraction that poly-Si having an average crystal grain diameter of approximately 1000 Å is deposited even though a film thickness of poly-Si is 1000 which is comparatively thin. In addition, X-ray diffraction peaks of crystal orientations are observed at (111) and (220) orientations, and especially, a poly-Si thin film which has a preferred orientation of {220} orientation is obtained. Further, a "preferred orientation of (hkl) orientation" here indicates a case such as O(hkl)>0.5 in crystalline orientation factor O(hkl) defined by formula 2.

[0018]

[chem. 2]

$$O(hkl)=I(hkl)/\Sigma_{hkl}I(hkl) \qquad \text{(formula 2)}$$

Here, I(hkl) indicates an object in which X-ray diffraction intensity from a {hkl} face is standardized by a film thickness of a sample and a X-ray scattering angle. In other words, Ihkl can be given by formula 3 in the case where X-ray diffraction intensity from the {hkl} face is i(hkl) and 2θ is a scattering angle.

[0019]

[chem. 3]

$$I(hkl)=i(hkl)/(1-\exp(-2\mu t/\sin\theta)) \qquad \text{(formula 3)}$$

Here, μ indicates an inverse number of an absorption coefficient of CuKα ray of silicon, and t indicates a film thickness.

[0020] In the case of using a halogen-based gas for an etching gas, thinning a film is

difficult since it is known that poly-crystallization begins from a film thickness of 2500 Å or more; however, there is an extraordinary effect on an application of a TFT according to the manufacturing method of the invention since thinning a film of poly-Si can be carried out.

[0021] The poly-Si deposited as above is patterned into a shape of a channel region 103 (FIG. 2-(b)). Subsequently, SiO_2 104 of a gate insulating film is deposited thereover to be approximately from 500 to 1500 Å (FIG. 2-(c)). A magnetron sputtering method in a mixed gas of $Ar+O_2$ atmosphere is preferable as a deposition method since SiO_2 which is superior in a film chamber (sic) can be obtained at a low temperature of a substrate temperature=approximately 200°C. The mixing ratio of Ar and O_2 is preferably $O_2/(Ar+O_2)$=approximately 0.3. High-quality SiO_2 can be obtained in a low temperature also by an electronic cyclotron resonance plasma CVD method. In addition, the gate insulating film may be a silicon nitride film by a PCVD method.

[0022] Then, a metal such as Cr or Mo/Ta or Al which is to be a gate electrode 105 is deposited by sputtering or the like at a temperature of from room temperature to approximately 300°C and is patterned (FIG. 2-(d)). The gate electrode may be doped poly-Si by a PCVD method. And then, SiO_2 106 of an interlayer insulating film is deposited to be approximately from 5000 to 8000 Å (FIG. 2-(e)). A contact hole is opened, and finally, metal (Al or the like) of a wiring electrode is deposited to be approximately 7000 Å and then patterned to be a source electrode 106 (sic) and a drain electrode 107 (sic); and thus, a TFT is completed (FIG. 2-(f)).

[0023] Electron field-effect mobility μ of a poly-SiTFT of the invention is 40 cm^2/Vs in the case of an n-channel and 20 cm^2/Vs in the case of a p-channel. On the contrary, μ of a conventional poly-SiTFT in which crystalline orientation rate of {110} orientation is less than 50% and an average crystal grain diameter is approximately 1000 Å is 15 cm^2/Vs in the case of an n-channel and 10 cm^2/Vs in the case of a p-channel. TFT mobility can be increased by aligning crystalline orientation into a {110} orientation.

[0024]

[Effect of the Invention] Electron field-effect mobility of a TFT can be heightened by making a TFT with a film in which crystal orientation of poly-Si is preferred oriented in {110} orientation as in this example. Further, there is no matter with mixing a halogen atom having an adverse effect on a TFT characteristic into a film since an etching gas which is used when poly-Si is deposited is hydrogen. In addition, poly-Si obtained by a conventional LPCVD method, a solid-phase growth method, a laser annealing method, or the like has a problem that an electric characteristic is deteriorated since there is a dangling bond in its crystalline grain boundary, and to solve the problem, passivation to a dangling bond is required by hydrogen plasma or the like after depositing poly-Si. However, a poly-Si thin film according to the method of the present invention is already exposed to hydrogen plasma at the time of depositing; therefore, there is an advantage that hydrogen passivation is not required to be performed later.

[0025] As described above, the invention has a profound effect on an application to a semiconductor element in general such as three dimensional SOI element in addition to a liquid crystal panel in which a large-size and high resolution are required, a driver circuit built-in type contact type image sensor, a load element for a high-integrated SRAM of 4 Mbit or more.

[Brief description of the Drawings]

[FIG. 1] A schematic view of a PCVD device used in the present invention.

[FIG. 2] A process drawing showing a manufacturing process of a thin film transistor of the invention.

[Description of Reference Number]

1 reaction chamber
2 exhaust duct
3 counter electrode
4 gas-blowout hole
5 gas-introducing portion
6 high frequency application electrode
7 heater for heating substrate
8 substrate

9	high frequency power source
100	substrate
101	source region
102	drain region
103	channel region
104	gate insulating film
105	gate electrode
106	interlayer insulating film
107	source electrode
108	drain electrode